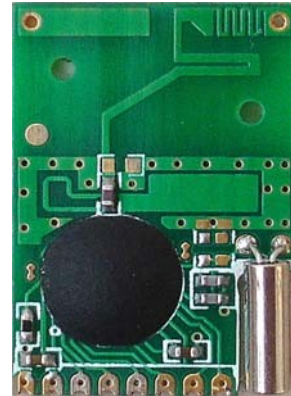
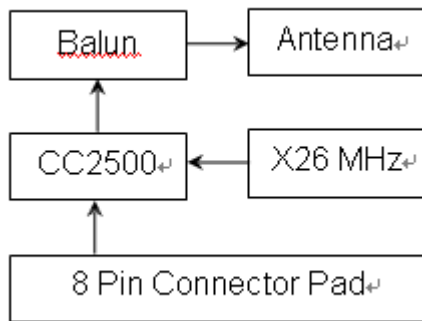


RCT03CC2501

邦定的 2.4G 无线数传模块

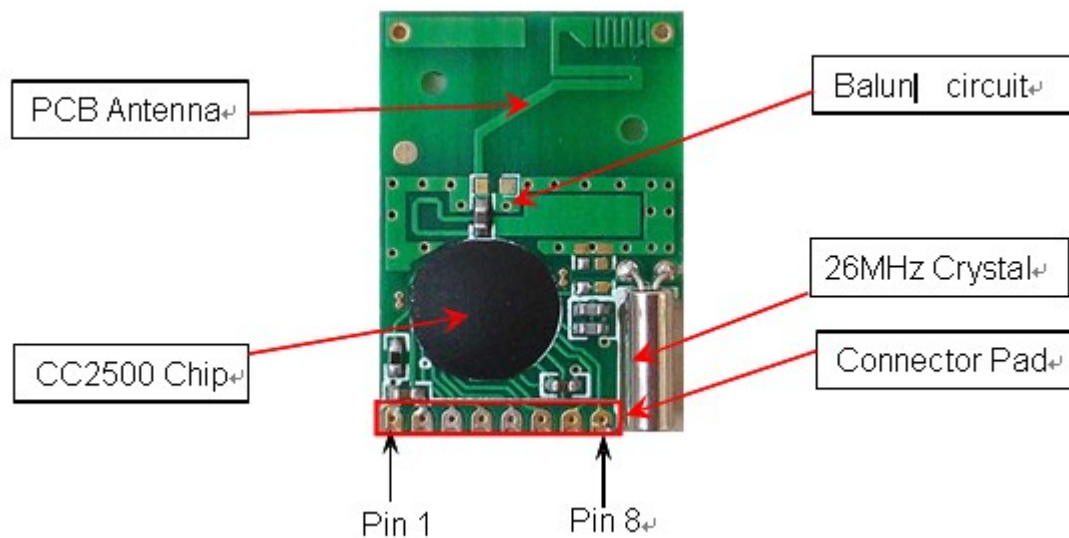
System Diagram



Applications

- 2400-2483.5 MHz ISM/SRD band systems
- Consumer electronics
- Wireless game controllers
- Wireless audio
- Wireless keyboard and mouse
- RF enabled remote controls

Module View



Pin Configuration

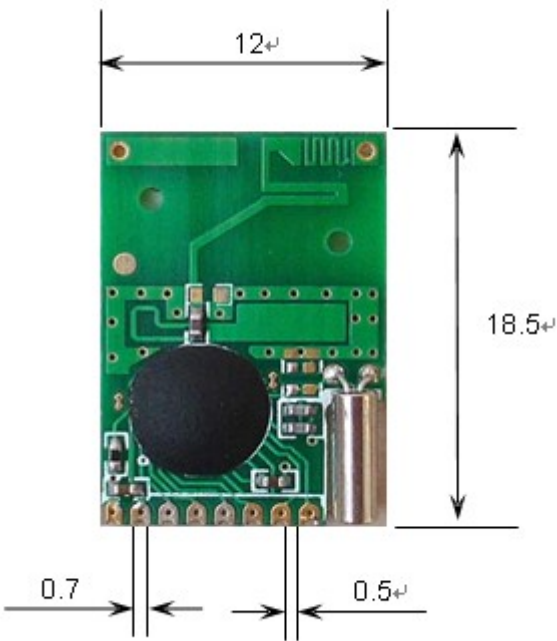
Pin	Symbol	Function
1	RFMOD_GND	Ground
2	RFMOD_VDD	RF module supply voltage
3	SI	serial configuration interface,data input
4	SCLK	serial configuration interface,clock input
5	SO	serial configuration interface,data output
6	GDO2	clock output
7	Rx/Tx Data(GDO0)	serial output Rx data/serial input Tx data
8	CSn	serial configuration interface,chip select

Operating Range

Parameters	Min	Max	Unit
Supply Voltage	1.8	3.6	V
Temperature ambient	0	60	°C

Mechanical Specification

Mechanical Specification				
	MAX	Typ	MIN	Unit
Width		12		mm
Length		18.5		mm
Height		2.2		mm
Pad Clearance		0.5		mm
Pad width		0.7		mm



Absolute Maximum Ratings

Under no circumstances must the absolute maximum ratings (given in below) be violated. Stress exceeding one or more of the limiting values may cause permanent damage to the device.				
Parameter	Min	Max	Unit	Condition
Supply voltage	- 0.3	3.9	V	All supply pins must have the same voltage
Voltage on any digital pin	- 0.3	VDD+0.3, max 3.9	V	
Voltage on the pins RF_P, RF_N and DCOUPL	- 0.3	2.0	V	
Voltage ramp-up rate		120	kV/ μ	
Input RF level		+10	dBm	
Storage temperature range	-50	150	°C	
Solder reflow temperature		260	°C	According to IPC/JEDEC J-STD-020D
ESD		<500	V	According to JEDEC STD 22, method A114, Human Body Model

Electrical Specification

Tc=25°C ,RFMOD_VDD=3V if nothing else stated						
NO	Parameters	Min	Typ	Max	Unit	Condition
1	Supply					
1.1	supply voltage	1.8		3.6	V	
2	Current consumption					
2.1	power down mode		2		μ A	
2.2	Idle mode		2		mA	
2.3	Rx states		20		mA	
2.4	Tx states		23		mA	
3	Transmitter Part					
3.1	Tx data rate		250		Kbps	
3.2	Frequency range	2400		2483.5	MHz	
3.3	Output power		-5		dBm	
3.4	Spurious emissions					
	25MHz-1GHz		-36		dBm	
	47-74,87.5-118,174-230,470-862MHZ		-54		dBm	
	1800-1900MHz		-47		dBm	
	At 2-RF and 3-RF		-41		dBm	
	Otherwise above 1GHz		-30		dBm	
4	Receiver Part					

4.1	Receiver sensitivity		-80①		dBm	
4.2	Receiver distance (hollowness place)		80		m	
4.3	Receiver channel filter bandwidth		541		KHz	
4.4	IF frequency		228.5		KHz	
4.5	Saturation		-13		dBm	
4.6	Adjacent channel rejection		21		dB	Desired channel 3 dB Above the sensitivity limit. 750kHz channel spacing
4.7	Alternate channel rejection		30		dB	Desired channel 3 dB Above the sensitivity limit. 750kHz channel spacing

Note: ① Receiver sensitivity measurement result obtain using the under setup
250KBaud data rate, sensitivity optimized, MDMCFG2.DEM_DCFILT_OFF=0
(MSK,1%packet error rate,20 bytes packet length,540KHZ digital channel filter bandwidth)

Analog Temperature Sensor

The characteristics of the analog temperature sensor at 3.0 V supply voltage are listed in below. Note that it is necessary to write 0xBF to the PTEST register to use the analog temperature sensor in the IDLE state.

Parameter	Min	Typ	Max	Unit	Condition/Note
Output voltage at -40°C		0.654		V	
Output voltage at 0°C		0.750		V	
Output voltage at +40°C		0.848		V	
Output voltage at +80°C		0.946		V	
Temperature coefficient		2.43		mV/°C	Fitted from -20°C to +80°C
Error in calculated temperature, calibrated	-2	0	2	°C	From -20°C to +80°C when using 2.43 mV / °C, after 1-point calibration at room temperature * The indicated minimum and maximum error with 1-point calibration is based on measured values for typical process parameters
Current consumption increase when enabled		0.3		mA	

DC Characteristics

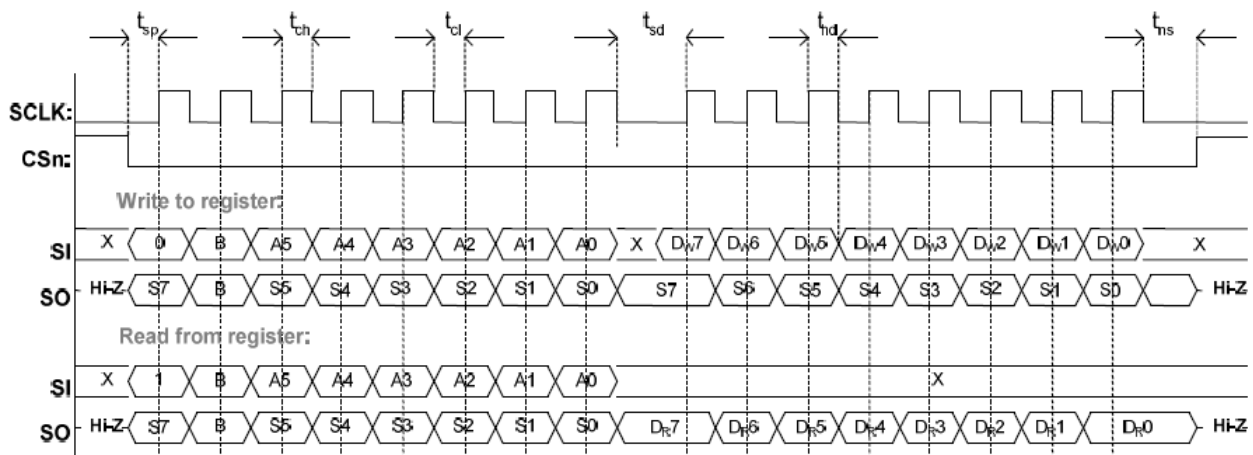
Tc = 25°C if nothing else stated.				
Digital Inputs/Outputs	Min	Max	Unit	Condition
Logic "0" input voltage	0	0.7	V	
Logic "1" input voltage	VDD-0.7	VDD	V	
Logic "0" output voltage	0	0.5	V	For up to 4 mA output current
Logic "1" output voltage	VDD-0.3	VDD	V	For up to 4 mA output current
Logic "0" input current	N/A	- 50	nA	Input equals 0 V
Logic "1" input current	N/A	50	nA	Input equals VDD

Power-On Reset

When the power supply complies with the requirements in below, proper Power-On-Reset functionality is guaranteed. Otherwise, the chip should be assumed to have unknown state until transmitting an SRES strobe over the SPI interface. See datasheets of CC2500 for further details.

Parameter	Min	Typ	Max	Unit	Condition/Note
Power ramp-up time			5	ms	From 0 V until reaching 1.8 V
Power off time	1			ms	Minimum time between power-on and power-off

Configuration Register Write and Read Operations



SPI Interface Timing Requirements

Param	Description	Min	Max	Units	
fSCLK	SCLK frequency 100 ns delay inserted between address byte and data byte (single access), or between address and data, and between each data byte (burst access).		10	MHz	
	SCLK frequency, single access No delay between address and data byte		9	MHz	
	SCLK frequency, burst access No delay between address and data byte, or between data bytes		6.5	MHz	
tsp,pd	CSn low to positive edge on SCLK, in power-down mode	150		μs	
tsp	CSn low to positive edge on SCLK, in active mode	20	-	ns	
tch	Clock high	50	-	ns	
tcl	Clock low	50	-	ns	
trise	Clock rise time	-	5	ns	
tfall	Clock fall time	-	5	ns	
tsd	Setup data (negative SCLK edge) to positive edge on SCLK (tsd applies between address and data bytes, and between data bytes)	Single access	55	-	ns
		Burst access	76	-	ns
thd	Hold data after positive edge on SCLK	20	-	ns	
tns	Negative edge on SCLK to CSn high	20	-	ns	